REMARKS

Applicants would like to thank the Examiner for the thorough examination of the present application. Independent Claims 9, 15, 21, 29 and 36 have been amended to address the 35 U.S.C. §112 informalities raised by the Examiner in order to advance prosecution of the present application. Other noted minor informalities have also been corrected in the claims. In addition, the equation on page 6, line 8 of the specification has been changed as helpfully noted by the Examiner. The arguments and claim amendments supporting patentability of the claims are presented in detail below.

I. The Claims Are Definite

The Examiner rejected independent Claims 9-37 and 40 as being indefinite under 35 U.S.C. §112 based upon the recitation "said first and second resistances having a same technology type." Independent Claims 9, 15, 21, 29 and 36 have been amended so that "a same technology type" is no longer recited therein.

Instead, the independent claims have been amended to recite that the respective integrated circuit voltage ramp generator/current ramp generator is produced using "CMOS" technology. In particular, the claims have been further amended to recite that the charging circuit is a "CMOS" charging circuit. Support in the specification may be found on page 4, lines 26-29, which provides:

> "According to the preferred embodiment of the invention, the components forming the voltage ramp generator and the current ramp generator are produced using CMOS technology." (Emphasis added.)

The specification thus discloses that the components of the voltage ramp generator and the current ramp generator are produced using CMOS technology. The Applicants submit that the claims are definite.

II. The Claims Are Patentable

The Examiner rejected independent Claims 9, 15, 21, 29 and 36 over the Applicants' prior art FIG. 1 in view of the Tanigawa patent and in view of the Lauffenburger patent.

The present invention, as recited in amended independent Claim 9, for example, is directed to an integrated circuit voltage ramp generator produced using CMOS technology. The integrated circuit voltage ramp generator comprises a capacitance, and a CMOS charging circuit connected to the capacitance. The CMOS charging circuit comprises a current generator having a first resistance, and a circuit connected to the current generator and to the capacitance. The circuit has a second resistance and enables a capacitance charging current to be proportional to a square of a ratio of the second resistance and the first resistance.

Since the integrated circuit voltage ramp generator is produced using CMOS technology, the respective spreads of the first and second resistances may be more easily compensated. The respective spreads may be due to operating temperature changes, for example. As discussed on page 7, lines 11-24 of the specification, the second resistance may be chosen with a temperature variation coefficient of the same order of magnitude as that for the first resistance, for

example. This advantageously allows compensation for variations in temperature due to the first resistance.

Without the second resistance, the spread of the first resistance may be reflected in variations of the capacitance charging current. To compensate for the spread of the first resistance, the second resistance is thus included. The capacitance charging current may also be controlled based upon the ratio of the second and first resistances. In particular, "the capacitance charging current is proportional to a square of a ratio of the second resistance and the first resistance," as recited in independent Claim 9.

Referring now to the Applicants' prior art FIG. 1, a ramp generator is disclosed as having a current source **Ig1** with no expressed teaching of the structure thereof. The Examiner cited Tanigawa as disclosing in FIG. 4 a current sink comprising "a current mirror" which has the advantage of gain control. The Examiner has taken the position that it would have been obvious to modify the current sink as disclosed in Tanigawa to a current source, and replace the current source **Ig1** in the Applicants' prior art FIG. 1 with the modified current source for obtaining a constant current with gain control.

Moreover, the Examiner has further taken the position that it would have been obvious to replace the bipolar transistors in Tanigawa with MOS transistors, and consequently, the current passing through transistor **Q1** of Tanigawa has a square element - just like the current passing through transistor **T5** (FIG. 2 in Applicants' specification) as indicated by the equation on page 6, line 11 of the Applicants' specification.

The Examiner further contends that since a diode-connected MOS transistor has a gate-to-source voltage effectively equal to the threshold voltage thereof, the difference in VGST-Vth must be negligible, as for transistor **T4** discussed on pages 5 and 6 of the Applicants' specification. Thus, regardless of the value of resistance Re, it must also be true that Re x Ig2 >> VGT-Vth (equation on page 6, line 6 of the Applicants' specification) for elements **9** and **Q2** of Tanigawa. Consequently, the Examiner contends that modification of the Applicants' prior art FIG. 1 in view of the Tanigawa patent results in "the capacitance charging current being proportional to a square of a ratio of the second resistance and the first resistance."

The Applicants submit that even if the references were selectively combined as suggested by the Examiner, the claimed invention is still not produced. In fact, Tanigawa teaches away from the claimed invention since the circuit illustrated in FIG. 4 is not suitable for semiconductor circuit integration.

First, in response to the Examiner's position stated above, the Applicants' respectfully submit that it is not necessarily true that Re x Ig2 >> VGST4-Vth4 for elements **9** and **Q2** of Tanigawa. According to the present invention, resistance **Re** is chosen so that Re x Ig2 >> VGST4-Vth4. By selecting the value of the second resistance (i.e., resistance **Re**), this leads to the "capacitance charging current being proportional to a square of a ratio of the second resistance and the first resistance," as in the claimed invention. Calculations supporting selection of resistance **Re** are provided on pages 6 and 7 of the Applicants' specification.

If the value of the second resistance **Re** is not chosen so that this equation is satisfied, then the claim recitation of the "capacitance charging current being proportional to a square of a ratio of the second resistance and the first resistance" is not achieved. Such a choice is not disclosed in Tanigawa. In other words, there is no current specification in Tanigawa, and regardless of the value of the resistance **Re**, it is not necessarily true that Re x Ig2 >> VGST4-Vth4 for elements **9** and **Q2** of Tanigawa.

Arguments with respect to the circuit illustrated in FIG. 4 of Tanigawa not being suitable for semiconductor circuit integration will now be provided. Independent Claim 9 has been amended to recite that the integrated circuit voltage ramp generator is produced using CMOS technology, and that the charging circuit is a CMOS charging circuit. The CMOS charging circuit includes the first and second resistances, and since these resistance are produced in CMOS technology, their respective spreads can be more readily compensated.

For instance, in CMOS integrated circuits, components typically have broad spreads. With respect to the current ramp generator illustrated in the Applicants' prior art FIG. 1, the spreads of resistors **Rg1** and **Rs** induce large variations of the gradient **ΔIs/Δt**, as discussed on page 3, lines 5-14 in the background section of the Applicants' specification. As further discussed in the background section of the Applicants' specification, current ramp spreads are adjusted by adjusting the resistance **Rs** with memory points of the fuse type, as discussed on page 3, lines 15-24. This is a tedious and time consuming operation.

The second resistance in the claimed invention advantageously permits compensation for the variations of the first resistance. The gain control circuit illustrated in FIG. 4 of Tanigawa is a "conventional gain control circuit of the current mirror type." (column 1, lines 12-13). This gain control device is not suitable for semiconductor circuit integration. Reference is directed to column 1, line 65 through column 2, line 2 in Tanigawa, which provides:

> "However, since the variable resistor **R** is necessary to be connected to the emitter of the transistor **Q2** externally in the circuit shown in FIG. 4, an external leading terminal is required. Accordingly, the circuit of FIG. 4, as it is, is not suitable for semiconductor circuit integration." (Emphasis added.)

In other words, the resistance **R** in Tanigawa is not produced in semiconductor technology. This is in sharp contrast to the claimed invention which recites that the voltage ramp generator is produced using CMOS technology, including the first and second resistances therein.

The Examiner cited Lauffenburger as disclosing circuitry being integrated onto a single substrate. The Applicants respectfully submit that Lauffenburger fails to provide the deficiencies as noted above, particularly with respect to the capacitance charging current being proportional to a square of a ratio of the second resistance and the first resistance. In fact, Lauffenburger fails to even mention resistors or resistances with respect to generating a capacitance charging current. Therefore, even if the references were combined as suggested by the Examiner, the

claimed invention is still not produced. Moreover, Tanigawa teaches away from the claimed invention since the circuit illustrated in FIG. 4 is not suitable for semiconductor circuit integration.

It thus appears that the Examiner is using impermissible hindsight reconstruction to selectively modify the Applicants' prior art FIG. 1 in view of Tanigawa and Lauffenburger in an attempt to produce the claimed invention. The prior art references, individually or in combination, do not teach or suggest that 1) the first and second resistances in the integrated circuit voltage ramp generator are produced using CMOS technology, and that 2) the second resistance is chosen so that the capacitance charging current is proportional to a square of a ratio of the second resistance and the first resistance.

Accordingly, it is submitted that amended independent Claim 9 is patentable over the Applicants' prior art FIG. 1 in view of Tanigawa and Lauffenburger. Independent Claims 15, 21, 29 and 36 have been amended similar to independent Claim 9. In view of the patentability of the independent claims as discussed above, it is submitted that their dependent claims, which recite yet further distinguishing features, are also patentable over the prior art. Thus, these dependent claims require no further discussion herein.

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GARNIER ET AL.
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CONCLUSION

In view of the amendments to the claims and the arguments provided herein, it is submitted that all the claims are patentable. Accordingly, a Notice of Allowance is requested in due course. Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,

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